TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

In re application of:	Enrique Musoll Mario D. Nemirovsky
Serial No.:	09/616385
Filed:	07/14/00
Docket:	MIPS.0165-00-US
For:	METHODS AND APPARATUS FOR IMPROVING FETCHING AND DISPATCH OF INSTRUCTIONS IN MULTITHREADED PROCESSORS

Attached hereto is Form PTO-1449 listing documents believed relevant to the subject application. It is respectfully requested that the Examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims and return an initialed copy of each form to the undersigned.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 C.F.R. § 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b) or is available as a reference under 35 U.S.C. § 102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the alleged "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98, and the Manual of Patent Examining Procedures § 609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

A copy of each document is enclosed. Some of the documents may have markings thereon. No significance is intended to be attached to the markings.

Respectfully submitted,

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Date of Deposit 9-7-04. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA 22313.
By: Vicki J. Hogan

Substitute for form 1449A/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				**Application Number**	**09/616385**
				Filing Date	**07/14/00**
				First Named Inventor	**Enrique Musoll** **Mario D. Nemirovsky**
				Group Art Unit	2183
				Examiner Name	Eric Coleman
Sheet	1	of	2	Attorney Docket Number	MIPS.0165-00-US

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AA	"The PowerPC Architecture: A Specification for a New Family of RISC Processors", Second Edition, May 1994, pp.70-72, Morgan Kaufmann, San Francisco.	
	AB	MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
	AC	POTEL, M.J., "Real-time Playback in Animation Systems", Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp.72-77, San Jose, CA.	
	AD	ARM Architecture Reference Manual, 1996, pp.3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall.	
	AE	ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ(AR001/CONTENTS)	
	AF	MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp.10-66, 10-67, and 10-71, Motorola, Inc.	
	AG	DIFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEEE Micro, April 1992, pp.40-63, Vol. 12, No.2.	
	AH	KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp.7-106 and 7-107, Prentice hall, New Jersey.	
	AI	DIEFENDORFF, KEITH et al., "AltiVec Extension to PowerPC Accelerates Media Processing", March –April 2000, pp.85-95, IEEE Micro, Vol. 20, No.2.	
	AJ	PAI, VIJAY et al., "An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors", Proceedings of ASPLOS VII, October 1996, pp.12-23, ACM, Inc.	
	AK	FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp.210-211, IEEE.	

Examiner Signature		Date Considered	

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	AL	YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of CA, Santa Barbara dissertation, December 1995, Santa Barbara, CA.	
	AM	STEERE et al, "A Feedback-Driven Proportion Allocator for Real Estate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp.145-158, USENIX Association.	
	AN	YAMAMOTO, WAYNE, et al., "Increasing Superscalar Performance Through Multistreaming", 1995.	
	AO	TULLSEN, DEAN, et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita, Ligure, Italy.	
	AP	YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp.42-53. IEEE.	
	AQ	KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of –Order Execution at 600 Mhz", August 1998.	
	AR	TULLSEN, et al., "Supporting Fine-Grained synchronization on a Simultaneous Multithreading Processor, UCSD CSE Technical Report CS98-587, June 1998, all pages, US.	
	AS	NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998.	
	AT	LI et al, "Design and Implementation of a Multiple-Execution-Pipeline Architecture", 7th International Conference on Parallel and Distributed Computing and Systems, October 1995.	
	AU	DONALSON et al., "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance", 26th Hawaii Conference on Systems Sciences, 1993, pp. 448-456, volume 1.	
	AV	NEMIROVSKY et al., "DISC: Dynamic Instruction Stream Computer ACM, 1991, pp. 163-171.	
	AW	YAMAMOTO, WAYNE et al, "Performance Estimation of Multistreamed, Superscalar Processors", IEEE, 1994, pp. 195-204, Hawaii, US	
	AX	GRUENWALD, et al., "Towards Extremely Fast Context Switching in a Block-Multithreaded Processor", Proceedings of EUROMICRO – 22, 1996, pp. 592-599	
	AY	BRADFORD, JEFFREY et al., "Efficient Synchronization for Multithreaded Processors", Workshop on Multithreaded Execution, Architecture and Compilation, January-February 1998, pp.1-4.	

Examiner Signature		Date Considered	